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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/758,083	METZLER, RICHARD A.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *39-41* is/are allowed.

6)☒ Claim(s) *1-5,7-38,42,43 and 45* is/are rejected.

7)☒ Claim(s) *44 and 46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/11/04&7/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 10, 12, 25, 27, 36, 38, 44 and 46 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10, 12, 25, 27, 36, 38, 44 and 46 are misdescriptive and rendered that claim indefinite, it is misdescritive to recite the transistor is p-channel transistor. Claim 1 recites that the anode of the diode is connected to the drain of the transistor. The recitation of claim 1 is read on to figures 3 and 5 that comprise n-channel transistor. However, the recitation of claim 1 does not read on figure 6 which comprises p-channel transistor because figure 6 shows the cathode, not anode of the diode is connected to the drain of the p-channel transistor.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 7, 9, 10, 13-18, 23-25 and 28-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Lacovella (FR 2612022).

As to claim 1, Lacavella discloses in figure 5 an integrated circuit having an on chip power supply coupled to a field effect transistor having a source (s), a drain (d), and a gate (g),

the power supply comprising: a charge storage device (C) and a current directing device (the diode); a first terminal of the charge storage device being connected to the source of the field effect transistor, a second terminal of the charge storage device being connected to a cathode of the current directing device, and an anode of the current directing device being connected to the drain of the transistor.

As to claim 2, figure 5 shows that the charge storage device is a capacitor.

As to claim 3, figure 5 shows that the current directing device is a diode.

As to claim 4, figure 5 shows that a voltage between the first and second terminals of the charge storage device is used to power a control circuit (R, Z).

As to claim 5, figure 5 shows that the control circuit is used to drive the gate of the transistor.

As to claim 7, figure 5 shows that a body of the field effect transistor is connected to the source, and the control circuit is responsive to a gate control signal to turn the field effect transistor on and off.

As to claim 9, figure 5 shows that the field effect transistor is an n-channel MOSFET.

As to claim 10, page 1, lines 16-20, teaches that the transistor can be a p-channel MOSFET.

As to claim 13, figure 5 shows that the field effect transistor functions as a rectifying diode.

As to claim 14, figure 5 shows an integrated circuit comprising: a capacitor (C); a diode; a field effect transistor having first (s) and second (d) terminals and a control terminal (g); the capacitor and the diode being connected in series between the first and second terminals of the

transistor; a control circuit (R, Z) coupled to the capacitor and to the control terminal; the charge in the capacitor being used to power the control circuit controlling the voltage on the control terminal of the transistor.

As to claim 15, figure 5 shows that the control circuit is responsive to the voltage between the first and second terminals of the transistor.

As to claim 16, figure 5 shows that the control circuit is configured to control the voltage on the control terminal to turn on the transistor when the voltage between the first terminal and the second terminal is of a first polarity and to turn off the transistor when the voltage between the first terminal and the second terminal is of a second polarity opposite the first polarity, the current directing device being conductive when the voltage between the first terminal and the second terminal is of the second polarity.

As to claim 17, figure 5 shows that the first terminal is a source, the second terminal is a drain and the control terminal is a gate, the gate being connected to the control circuit.

As to claim 18, figure 5 shows that the circuit is packaged as a two terminal device.

As to claim 23, figure 5 shows that the transistor is a FET.

As to claim 24, figure 5 shows that the FET is an n-channel MOSFET.

As to claim 25, page 1, lines 16-20, teaches that the FET is a p-channel MOSFET.

As to claim 28, figure 5 shows that the field effect transistor functions as a rectifying diode.

As to claim 29, figure 5 shows a circuit comprising: an integrated circuit including a charge storage device (C), a current directing device (the diode), a field effect transistor having a body, a source (s), a drain (d) and a gate (g), and a control circuit (R, Z), the charge storage

device and the current directing device being connected in series between the source and drain terminals of the transistor, a charge on the charge storage device being coupled to and acting as the power supply for the control circuit, the control circuit having an output coupled to the gate of the field effect transistor, the control circuit turning the transistor on when the voltage between the source and drain is of a first polarity, and off when the voltage between the source and drain is of a second polarity, the current directing device having a polarity to charge the charge storage device when the voltage between the source and drain is of a second polarity.

As to claim 30, figure 5 shows that the charge storage device is a capacitor.

As to claim 31, figure 5 shows that the current directing device is a diode.

As to claim 32, figure 5 shows that the field effect transistor is an integrated circuit diode having its gate connected to the control circuit.

As to claim 33, figure 5 shows that the circuit is packaged as a two terminal device.

As to claim 34, figure 5 shows that the transistor is a FET.

As to claim 35, figure 5 shows that the FET is an n-channel MOSFET.

As to claim 36, page 1, lines 16-20, teaches that the FET is a p-channel MOSFET.

5. Claims 1-5, 7-9, 14-17, 19-24, 29-31, 34, 35, 42 and 43 are rejected under 35 U.S.C. 102(b) as being anticipated by Tago et al. (JP 10-215568).

As to claim 1, Tago et al. discloses in figure 1 an integrated circuit having an on chip power supply coupled to a field effect transistor (Q1) having a source (s), a drain (d), and a gate (g), the power supply comprising: a charge storage device (the capacitor in circuit 3) and a current directing device (the diode in circuit 3); a first terminal of the charge storage device being connected to the source of the field effect transistor, a second terminal of the charge

storage device being connected to a cathode of the current directing device, and an anode of the current directing device being connected to the drain of the transistor.

As to claim 2, figure 1 shows that the charge storage device is a capacitor.

As to claim 3, figure 1 shows that the current directing device is a diode.

As to claim 4, figure 1 shows that a voltage between the first and second terminals of the charge storage device is used to power a control circuit (4).

As to claim 5, figure 1 shows that the control circuit is used to drive the gate of the transistor.

As to claim 7, figure 1 shows that a body of the field effect transistor is connected to the source, and the control circuit is responsive to a gate control signal to turn the field effect transistor on and off.

8. The circuit of claim 7 wherein the circuit is packaged as a three terminal device.

As to claim 9, figure 1 shows that the field effect transistor is an n-channel MOSFET.

As to claim 14, figure 1 shows an integrated circuit comprising: a capacitor (the capacitor in circuit 3); a diode (in circuit 3); a field effect transistor (Q1) having first (s) and second (d) terminals and a control terminal (g); the capacitor and the diode being connected in series between the first and second terminals of the transistor; a control circuit (4) coupled to the capacitor and to the control terminal; the charge in the capacitor being used to power the control circuit controlling the voltage on the control terminal of the transistor.

As to claim 15, figure 1 shows that the control circuit is responsive to the voltage between the first and second terminals of the transistor.

As to claim 16, figure 1 shows that the control circuit is configured to control the voltage on the control terminal to turn on the transistor when the voltage between the first terminal and the second terminal is of a first polarity and to turn off the transistor when the voltage between the first terminal and the second terminal is of a second polarity opposite the first polarity, the current directing device being conductive when the voltage between the first terminal and the second terminal is of the second polarity.

As to claim 17, figure 1 shows that the first terminal is a source, the second terminal is a drain and the control terminal is a gate, the gate being connected to the control circuit.

As to claim 19, figure 1 shows that the control circuit is responsive to a control signal (output of 7) provided thereto.

As to claim 20, figure 1 shows that the circuit is packaged as a three terminal device.

As to claim 21, figure 1 shows that the control circuit is configured to control the voltage on the control terminal responsive to the control signal to provide enhanced turn on of the transistor responsive to a transistor turn-on control signal.

As to claim 22, figure 1 shows that the current directing device is oriented to provide charging current to the charge storage device when the transistor is turned off.

As to claim 23, figure 5 shows that the transistor is a FET.

As to claim 24, figure 5 shows that the FET is an n-channel MOSFET.

Claims 29-31, 34 and 35 recite similar to claims above. Therefore, they are rejected for the same reasons.

As to claim 42, figure 1 shows a circuit comprising: an integrated circuit including: a capacitor (capacitor in circuit 3); a diode; a field effect transistor (Q1) having a source (s), a

drain (d), a gate (g) and a body connected to the source; and, a control circuit (4); the capacitor and the diode being connected in series between the source and drain with the diode being conductive to charge the capacitor when the transistor is turned off, the capacitor being coupled to and acting as the power supply for the control circuit, the control circuit having a gate control input (input of 4) and providing an output coupled to the gate of the field effect transistor to provide an enhanced gate control signal to the field effect transistor responsive to the gate control input.

As to claim 43, figure 1 shows that the field effect transistor is an n-channel MOSFET.

As to claim 47, figure 1 shows that the circuit is packaged as a three terminal device.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 11, 12, 26, 27, 37, 38 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lacovella (FR 2612022) or Tago et al (JP 10-215568) in view of Yu (USP 6566936).

Lacovella or Tago et al. reference shows all limitations of the claims except for the transistor is JFET. However, Yu teaches in column 1, lines 47-52, that JFET is used as switch circuit for its high speed advantage. Therefore, it would have been obvious to one having ordinary skill in the art to use JFET to Lacovella and Tago et al.'s transistors for the purpose of improving the circuit's speed.

Allowable Subject Matter

8. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 44 and 46 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

10. Claims 39-41 are allowed.

Claim 6 would be and claims 39-41 are allowable because the prior art fails to teach the body of the transistor is connected to its drain with the combination of elements as claimed.

Claim 44 and 46 would be allowable because the prior art fails to teach the transistor is p-channel transistor with the combination of elements as recited.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Primary Examiner

February 14, 2005